G65SC32

Microcircuits

CMOS RAM, I/O, Timer

Features

- CMOS process technology for low power consumption
- Fully compatible with NMOS 6532 devices
- Bus compatible with 6500 and 6800 microprocessors
- Low power consumption (2 mA at 1 MHz)
- 128 X 8 bit static RAM
- Two 8-bit bidirectional peripheral data ports
- Two programmable Data Direction Registers
- Programmable Edge Sense Interrupt function
- Interrupt Timer with programmable interrupt intervals
- Peripheral I/O Port B allows direct transister drive
- High impedance three-state Data Bus
- Available in 40-pin dual-in-line package

General Description

The G65SC32 is a programmable RAM, I/O, Timer device for use with the G65SCXXX series 8-bit microprocessor family. The G65SC32 includes functions for programmed control of up to two peripheral devices (Port A and Port B). These functions include:

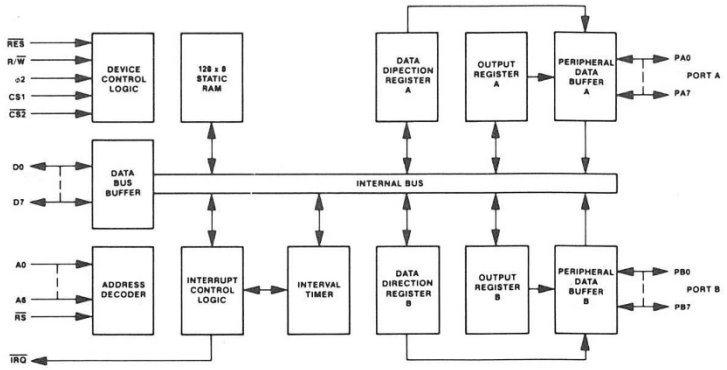
- 128 X 8 bit static RAM for microprocessor scratch pad activity.
- Two program controlled 8-bit bidirectional Data Ports for direct interfacing between the microprocessor and selected peripheral units.
- Two programmable Data Direction Registers (A and B) for data direction control at each peripheral Data Port.
- A programmable Interrupt Timer with interrupt timing capability in intervals ranging from 1 to 262,144 clock periods.
- Edge-detect interrupt circuitry for interrupt generation on active edge transitions.

The G65SC32 offers the many advantages of GTE's leading edge CMOS technology, i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

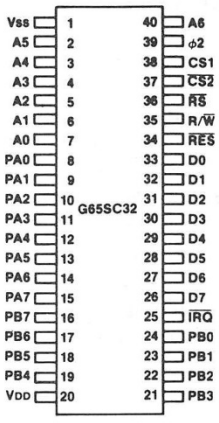
Pin Function Table

A0-A6	Address Bus	$\overline{RS}$	Function Select
D0-D7	Data Bus	R/$\overline{W}$	Read/Write
PA0-PA7	Peripheral I/O Port A	$\overline{RES}$	Reset
PB0-PB7	Peripheral I/O Port B	$\overline{IRQ}$	Interrupt
ϕ2	Phase 2 Internal Clock	VDD	Power Supply (+5V)
CS1/$\overline{CS2}$	Device Select	VSS	Internal Logic Ground

Block Diagram



Pin Configuration



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to V_{DD} + 0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these rating may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, A0-A6, ϕ2, CS1, $\overline{CS2}$, R/$\overline{W}$, $\overline{RES}$, $\overline{RS}$)	I_{IN}		±1.0	μA
Three-State, Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, $\overline{IRQ}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7	I_{IL}		1.6	mA
Output Low Voltage (I_{OL} = 3.2 mA), D0-D7, PA0-PA7, PB0-PB7, $\overline{IRQ}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), D0-D7, PA0-PA7, PB0-PB7, $\overline{IRQ}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz	I_{DD}		2.0	mA
f = 2 MHz	I_{DD}		4.0	mA
f = 3 MHz	I_{DD}		6.0	mA
f = 4 MHz	I_{DD}		8.0	mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz)	P_D		11.0	mW
Standby (Static)	P_{DSB}		11.0	μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

		G65SC32-1		G65SC32-2		G65SC32-3		G65SC32-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 1)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS
Write Timing (Figure 2)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay	t_{CPW}	—	1000	—	500	—	330	—	250	nS

Timing Diagrams

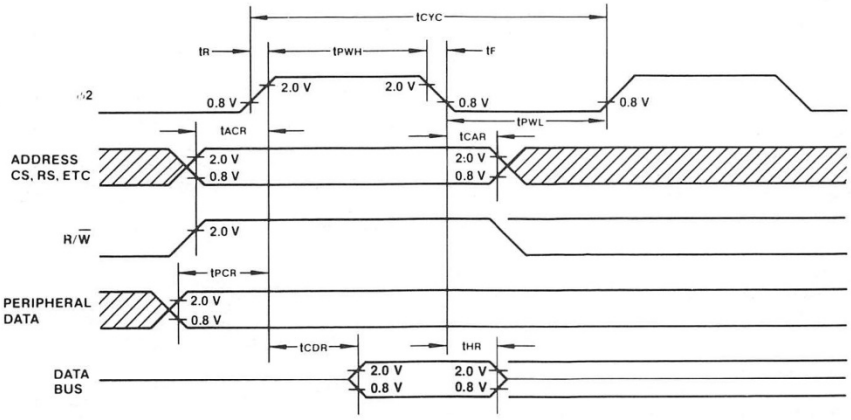


Figure 1. Read Timing

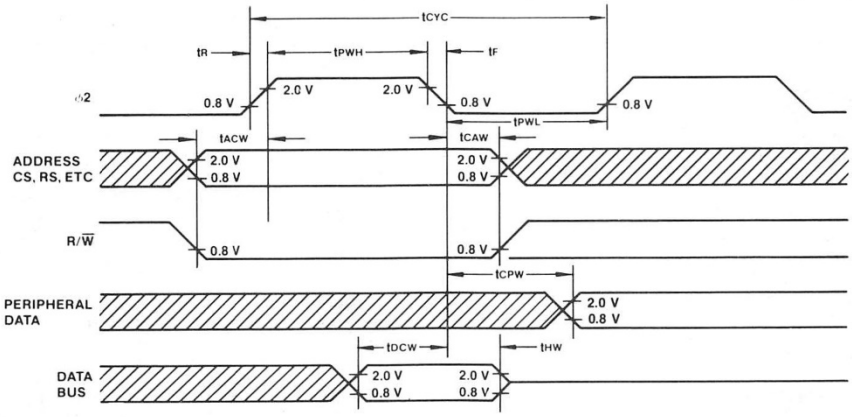
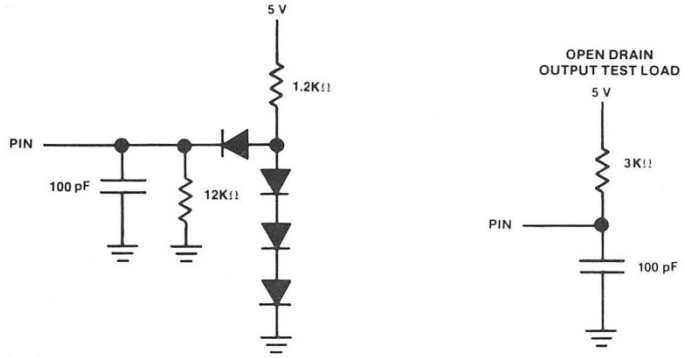


Figure 2. Write Timing

Test Load



Interface Signals

Input Clock ($\phi 2$)
The Input Clock consists of a system $\phi 2$ clock source. This clock can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or a high level clock ($V_{IL} < 0.2$, $V_{IH} = V_{DD} + 0.3$ "or" $V_{DD} - 0.2$).

Reset ($\overline{RES}$)
During system initialization a Logic "0" on the $\overline{RES}$ input will cause all four I/O registers to be zeroed. This in turn will cause all lines within the I/O bus to serve as inputs. This arrangement protects external components from possible damage and/or erroneous data being written during system configuration under software control. Also, the Data Bus Buffers are placed in an Off-State during any $\overline{RES}$. Interrupt capability is disabled during $\overline{RES}$. The $\overline{RES}$ signal must be held low for a minimum of one clock period during a $\overline{RES}$ function.

Interrupt Request ($\overline{IRQ}$)
The $\overline{IRQ}$ output signal is derived from the Interrupt Control Logic, and is normally in the high state (Logic "1"). When in the low state (Logic "0"), $\overline{IRQ}$ indicates an interrupt exists within the G65SC32. This interrupt output may be activated (Logic "0") by a logical transition on line PA7 of peripheral I/O Bus A, or by timeout of the Interval Timer. Interrupt Request is an open-drain output, thus allowing several units to be wire-ORed to a common microprocessor $\overline{IRQ}$ input pin.

Data Bus (D0-D7)
The G65SC32 contains eight bidirectional data lines (D0-D7) for transfer of data to and from the microprocessor. The Data Buffer is active during a Read operation, and is held in the Off-State during all other operations.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data to and from the G65SC32. When R/$\overline{W}$ is in the high state (Logic "1"), the microprocessor is allowed to read data from the G65SC32. Conversely, when R/$\overline{W}$ is in the low state (Logic "0"), the microprocessor may write data to the G65SC32. Read/Write functions must always be preceded by proper addressing.

Peripheral Data Ports (PA0-PA7 and PB0-PB7)
The G65SC32 contains two 8-bit peripheral I/O Ports... Port A (lines PA0-PA7) and Port B (lines PB0-PB7). An important feature of the G65SC32 is that each peripheral port bus line is individually programmable as either an input or an output. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. This feature is accomplished by the Data Direction Registers. When a "0" is written to any bit position of the Data Direction Register (DDRA or DDRB), the corresponding line will be programmed as an input. Likewise, when a "1" is written into any bit position of DDRA or DDRB, the corresponding data line will serve as an output.

When an I/O Port line has been programmed as an input and its Output Register (ORA or ORB) is read by the microprocessor, the TTL level on the I/O Port line will be transferred to the Data Bus (D0-D7). When programmed as outputs, the I/O Port lines will reflect data as written by the microprocessor into the Output Registers. I/O Port line PA7 also serves an Edge Sense Interrupt function as described in the following sections.

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)
Address lines A0-A6 serve to address the RAM, I/O Registers, Timer and Flag Register. CS1 and $\overline{CS2}$ are used to select (enable access to) the G65SC32.

Functional Description

In reference to the Block Diagram on page one, the G65SC32 is shown to consist of four basic functions; that is, RAM, I/O, Timer and Interrupt Control. RAM interfaces directly with the microprocessor by way of the Data Bus and Address Lines. The peripheral I/O functions consist of two 8-bit I/O Ports. Each port is supported by a Data Direction Register and an Output Register.

RAM (128 Bytes, 1024 Bits)
Within the G65SC32 is a 128 X 8 bit static RAM. This RAM is used as a scratch pad or special data buffer, and is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1 and $\overline{CS2}$.

Peripheral I/O Port Registers
The peripheral I/O Port Registers consist of two Data Direction Registers and two data Output Registers. The Data Direction Register (A and B) controls the direction of data into and out of the peripheral I/O Ports as described under the Peripheral Data Ports Section above. The voltage level on any I/O Port line which has been programmed as an output, is determined by the corresponding bit in the Output Register (ORA or ORB).

During a peripheral Read operation over I/O Port A, data is read directly from the I/O Port bus (PA0-PA7). During this Read operation, should a particular PA line be programmed as an output, data transferred into the microprocessor will be identical to the corresponding data in Output Register A providing that line loading is such that the line voltage is $\geq$ 2.4 volts for a Logic "1", and $\leq$ 0.4 volts for a Logic "0". Under severe loading conditions where these voltage limits cannot be guaranteed, the resulting Read operation may not match the contents of Output Register A.

The output buffer which services I/O Port B (PB0-PB7) is different from the buffers for I/O Port A. The buffers for Port B are push-pull devices capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To ensure valid data will be read during a peripheral Read operation, I/O Port B contains logic which allows the microprocessor to read the contents of Output Register B instead of reading directly from the Port B data bus.

Interval Timer
Figure 3 shows the three basic functions of the Interval Timer section. These functions include: a preliminary divide-down register, a programmable 8-bit register, and all necessary interrupt logic.

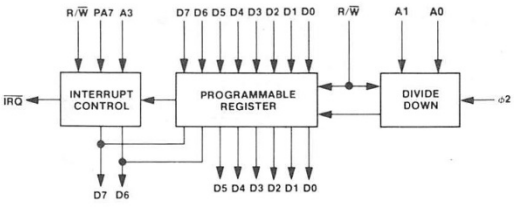


Figure 3. Basic Functions of Interval Timer

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be selected as 1T, 8T, 64T, or 1024T increments, where T is the system clock ($\phi 2$) period. When a full interval count has been reached, the interrupt flag is set to the Logic "1" state. Once the flag has been set, the internal clock starts counting down at a 1T rate to a maximum count of -255T. This arrangement allows the user to read the counter and thus determine the elapsed time since the interrupt was set.

The G65SC32's internal Data Bus is used to transfer data to and from the Interval Timer. For example, if a count of 52 time intervals is desired, the pattern 00110100 would be put on the Data Bus and written into the Interval Time Register. During the time when data is being written into the Interval Timer, timing intervals 1,8,64 and 1024T are decoded from address lines A0 and A1. During Read and Write operations, address line A3 controls the interrupt capability of $\overline{IRQ}$. That is, when A3=1, $\overline{IRQ}$ is enabled. When A3=0, $\overline{IRQ}$ is disabled. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read to or written from by the microprocessor. When $\overline{IRQ}$ is enabled by A3 and an interrupt occurs, $\overline{IRQ}$ will go low. Should the Timer be read prior to the interrupt flag being set, the number of remaining time intervals will be read, i.e., 51, 50, 49, etc.

Once the Timer has counted down to 00000000, an interrupt will occur on the next count time which will result in the Timer reading 11111111. Following the interrupt, the Timer registers decrements at a divide by "1" rate of the clock system. After interrupt, should the Timer read a value of 11100100, then the time since the last interrupt is 28T. The value read is in two's complement as follows:

Value read = 11100100
Complement = 00011011
Add 1 = 00011100 = 28T (28 $\phi 2$ clock periods)

Thus, to arrive at the total elapsed time since the Timer count was originally program set, simply perform a two's complement of the Timer value and add this to the original time value written into the Timer. For example, assume the original time written was 00110100 (=52). With a divide-by-8T, total time to interrupt would be (52 X 8) + 1 = 417T. In this case, total elapsed time would then be 416T + 28T = 444T, assuming the value read after interrupt was 11100100.

Following an interrupt, whenever the Timer is read or written the interrupt is reset. However, should the Timer be read at the same time the interrupt occurs, the interrupt flag will not reset. Figure 4 is an example of Timer Interrupt Timing.

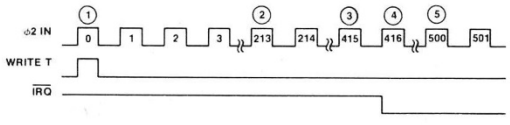


Figure 4. Timer Interrupt Timing

1. Data written into Interval Timers: $00110100 = 52_{10}$
2. Data in Interval Timer: $000110100 = 25_{10}$
   i.e., $52 - \frac{213}{8} - 1 = 52 - 26 - 1 = 25$
3. Data in Interval Timer: $00000000 = 0_{10}$
   i.e., $52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$
4. Interrupt occurred at $\phi 2$ clock pulse number 416
   Data in Interval Timer = 11111111
5. Data in Interval Timer: 10101100
   Two's complement: $01010100 = 84_{10}$
   Therefore, $84 + (52 \times 8) = 500_{10}$

When reading the timer following an interrupt, address line A3 must be low such that $\overline{IRQ}$ will be disabled. This procedure prevents future interrupts until a future Write operation has occurred.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits ... the Timer interrupt flag (bit 7) and the PA7 Edge Sense Interrupt flag (bit 6). Whenever a Read operation is performed on the Interrupt Flag Register, the two bits are transferred to the microprocessor via the internal Data Bus. Figure 5 shows the Interrupt Flag Register bit configuration.

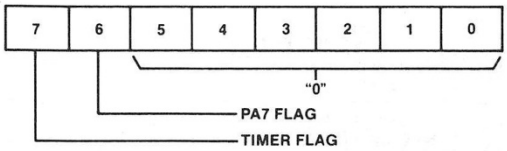


Figure 5. Interrupt Flag Register

It should be noted that the PA7 flag is cleared when the Interrupt Flag Register is read. Also, the Timer flag is cleared when the Timer is either read or written.

Addressing

The G65SC32 is addressed by way of the 7-bit Address Bus (A0-A6), the $\overline{RS}$ input, and the two Chip Select inputs (CS1 and $\overline{CS2}$). To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ both low. To address the I/O and Interval Timer, CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. It is apparent that in order to access the G65SC32 device, CS1 must be high and $\overline{CS2}$ must be low. The $\overline{RS}$ input is used to distinguish between the RAM and the I/O — Interval Timer Sections. When $\overline{RS}$ is low, RAM is addressed. When $\overline{RS}$ is high, the I/O — Interval Timer Section is addressed. To distinguish between Interval Timer and I/O, address line A2 is used. With A2 high, the Interval Timer is accessed. With A2 low, the I/O registers are accessed. Table 1 provides addressing requirements for the G65SC32.

MICRO-PROCESSORS

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can also function as an Edge Sense Interrupt input. In the interrupt mode, an active transition on line PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, providing the PA7 interrupt has been enabled, the $\overline{IRQ}$ output will go low.

Control of the PA7 edge detection logic is accomplished by a Write operation to one of four addresses. The data lines for this Write operation are "don't care" and the addresses to be used can be found in Table 1.

Setting the internal interrupt flag by an active transition on PA7 is always enabled, independent of whether PA7 is set up as an input or output by the Data Direction Register.

The Reset signal ($\overline{RES}$) will disable the PA7 interrupt and at the same time set the active transition logic to the negative edge-detect state. During the $\overline{RES}$ operation, the interrupt flag may be set by a negative transition of PA7. This being the case, it may therefore be necessary to clear the interrupt flag prior to being enabled for its normal use as an edge detecting input. This special Reset can be achieved by reading the Interrupt Flag Register.

I/O Register—Timer Addressing

Table 1 provides the address decoding for all internal functions and Timer programming. Address line A2 distinguishes the I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 may be used to address the desired register.

With A2 high and $\overline{RS}$ high, the Timer is selected, and address lines A1 and A0 are available to decode the "divide-by" matrix as defined in Table 1. Address line A3 is used to enable the interrupt flag to the $\overline{IRQ}$ output.

Address Decoding

Table 1. G65SC32 Address Decoding

Operation	$\overline{RS}$	R/$\overline{W}$	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Timer							
÷ 1T	1	0	1	(a)	1	0	0
÷ 8T	1	0	1	(a)	1	0	1
÷ 64T	1	0	1	(a)	1	1	0
÷ 1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

Notes: — = Don't Care, "1" = High Level ($\geq$ 2.4V), "0" = Low Level ($\leq$ 0.4V)

(a) A3 = 0 to Disable Interrupt from Timer to $\overline{IRQ}$
A3 = 1 to Enable Interrupt from Timer to $\overline{IRQ}$

(b) A1 = 0 to Disable Interrupt from PA7 to $\overline{IRQ}$
A1 = 1 to Enable Interrupt from PA7 to $\overline{IRQ}$

(c) A0 = 0 for Negative Edge-Detect
A0 = 1 for Positive Edge-Detect

Application Diagram